

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

**Title of
Invention**

CRITICAL AREA COMPUTATION OF COMPOSITE FAULT
MECHANISMS USING VORONOI DIAGRAMS

Application Number :

Confirmation Number:

First Named Applicant: Robert Allen

Attorney Docket Number: BUR920030136US1

Art Unit:

Examiner:

Search string: (6178539 or 6247853 or 6317859).pn

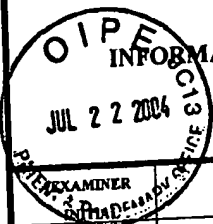
US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
SP	1	6178539	2001-01-23	Papadopoulou et al.			
SP	2	6247853	2001-06-19	Papadopoulou et al.			
SP	3	6317859	2001-11-13	Papadopoulou et al.			

Signature

Examiner Name	Date
<i>Sushin Parihar</i>	4-20-06

<div style="text-align: center;">  <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p> </div>		Docket Number (Optional) BUR920030136US1	Application Number 10/702293
		Applicant(s) Allen et al.	
		Filing Date 4-27-04	Group Art Unit Unknown
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
SR		Papadopoulos, E. and Lee, D.T., "Critical area computation via Voronoi diagrams," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Vol. 18, No. 4, pp .463-474, April 1999.	
SR		Papadopoulos, E., "Critical area computation for missing material defects in VLSI circuits," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Vol. 20, No. 5, pp 583-597, May 2001.	
SR		Fook-Luen Heng and Zhan Chen. "VLSI Yield Enhancement Techniques Through Layout Modification." IBM T. J. Watson Research Center, pp. 1-15, July 17, 2000.	
		A. Venkataraman and I. Koren. "Trade-offs between Yield and Reliability Enhancement." Proc. of the 1996 IEEE National Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 67-75, November 1996.	
EXAMINER <i>Sushin Parihar</i>		DATE CONSIDERED 4-20-06	
<p>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>			